Docket No.: 067471-0030

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Taketo Heishi et al.	:	Confirmation Number: 5444
Application No.: 10/720,030	:	Group Art Unit: 2183
Filed: November 24, 2003	:	Examiner: William Partridge

For: INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE

SUPPLEMENTAL DECLARATION IN REISSUE APPLICATION PURSUANT TO 37 C.F.R. § 1.175(b)

1. We, Taketo Heishi, Tetsuya Tanaka, Nobuo Higaki, Shuichi Takayama, and Kensuke Odani, all citizens of Japan, hereby declare that we are the original, first and joint inventors of the subject matter of U.S. Patent No. 6,324,639 (the '639 patent) entitled INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE, which issued November 27, 2001, from U.S. application Serial No. 09/280,777, filed March 29, 1999; that we were employed by Matsushita Electric Industrial Co., Ltd. of Osaka, Japan (now named Panasonic Corporation as the result of a corporate name change) at the time this Reissue application was filed; that Panasonic Corporation is the Assignee of the entire interest of this Reissue application; that at the time this Reissue application was filed we were engaged in the design of electronic technology and processors as described in the '639 patent; that we do not know and do not believe that the invention was ever known or used in the United States before our invention; and that we are the declarants, applicants and patentees, referred to hereinafter.

2. That we believe we are the original/first inventors of the subject matter of the invention, which is claimed and for which a reissue patent is sought in this Reissue application.

3. That we believe the '639 patent to be wholly or partly inoperative or invalid, by reason of our claiming less than we had a right to claim. Specifically, claims 1-33 fail to embody one of the inventive features of the present invention without undue limitations, e.g., an execution unit which executes up to N number of instructions having a variable bit length in parallel, with the maximum bit length of an instruction that is executed in parallel being M bits, and an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than M * N bits.

We believe this inventive concept is not disclosed or suggested by prior art so as to be patentable without further limitation; whereas claims in the '639 patent fail to embody this inventive concept without undue limitations, so that we claimed less than we had a right to claim.

4. That we believe that the error regarding our narrow claiming of the invention arose inadvertently and without deceptive intent.

5. That every error in the '639 patent which is corrected by this Reissue application, and is not covered by a prior oath/declaration submitted in this Reissue application, arose without any deceptive intent.

6. In accordance with 35 U.S.C. § 119, we claim the benefit of the foreign filing date of Japanese Patent Application No. 10-083368, filed on March 30, 1998 and Japanese Patent Application No. 10-095647, filed on April 8, 1998. A certified copy of the Japanese priority documents was filed in the parent application Serial No. 09/280,777 that issued as the '639 patent.

7. That we have reviewed and understand the contents of this Reissue application, including new claims 40-56 added by amendment, and all subsequent amendments made to these claims.

8. That we acknowledge the duty to disclose information of which we are aware and which is material to the patentability of this Reissue application in accordance with 37 C.F.R. § 1.56(a).

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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